WHAT IS CLAIMED IS:

1. A failure analysis method of a semiconductor device, comprising the steps of:

(a) in a fail bit map obtained from a semiconductor device including a plurality of memory cells arranged in a matrix, counting the number of failure bits with respect to each row of a region classified as a block failure;

(b) in said fail bit map, counting the number of failure bits with respect to each column of said region;

(c) finding a first threshold value from an average value of said number of failure bits with respect to each row, to compare said number of failure bits with respect to each row and said first threshold value;

(d) finding a second threshold value from an average value of said number of failure bits with respect to each column, to compare said number of failure bits with respect to each column and said second threshold value;

(e) after said step (c), calculating an average value of a result of comparison with respect to each row as an average value of rows;

(f) after said step (d), calculating an average value of a result of comparison with respect to each column as an average value of columns;

(g) determining that said semiconductor device contains a block failure in a column direction, a block failure in a row direction, or a random block failure, said block failure in a column direction satisfying a condition that said average value of rows is greater than a value obtained by multiplying said average value of columns by a predetermined factor, said block failure in a row direction satisfying a condition that said average value of columns is greater than a value obtained by multiplying said average

value of rows by said predetermined factor, said random block failure satisfying conditions that said average value of rows is not more than a value obtained by multiplying said average value of columns by said predetermined factor, and said average value of columns is not more than a value obtained by multiplying said average value of rows by said predetermined factor.

2. The failure analysis method according to claim 1, further comprising the steps of:

(h) dividing said fail bit map in a column direction, classified as said block failure in a column direction, into equal sections with respect to the certain number of columns;

(i) counting the respective numbers of failure bits existing in the same-numbered columns in all of said sections, to calculate the number of failure bits in each column of a group as an aggregate of said sections of columns; and

(j) finding a third threshold value from a maximum value of the number of failure bits in each column of said group, and comparing said third threshold value and the number of failure bits in each column, to extract a column having the number of failure bits greater than said third threshold value.

3. The failure analysis method according to claim 1, further comprising the steps of:

(k) dividing said fail bit map in a row direction, classified as said block failure in a row direction, into equal sections with respect to the certain number of rows;

(l) counting the respective numbers of failure bits existing in the same-numbered rows in all of said sections, to calculate the number of failure bits in each

row of a group as an aggregate of said sections of rows; and

(m) finding a fourth threshold value from a maximum value of the number of failure bits in each row of said group, and comparing said fourth threshold value and the number of failure bits in each row, to extract a row having the number of failure bits greater than said fourth threshold value.

4. The failure analysis method according to claim 2, further comprising the steps of:

(n) after said step (g), dividing said fail bit map in a row direction into equal sections with respect to the certain number of rows, and

(o) in each section, converting each column to one failure bit when said column contains the predetermined number of failure bits or more, and converting each column to one normal bit when said column contains the number of failure bits of less than said predetermined number, to form a fail bit map in which rows defining said section is compressed into one row.

5. The failure analysis method according to claim 3, further comprising the steps of:

(p) after said step (g), dividing said fail bit map in a column direction into equal sections with respect to the certain number of columns, and

(q) in each section, converting each row to one failure bit when said row contains the predetermined number of failure bits or more, and converting each row to one normal bit when said row contains the number of failure bits of less than said predetermined number, to form a fail bit map in which columns defining said section is compressed into one column.

6. The failure analysis method according to claim 1, further comprising the step of:

(r) previously defining an extent of said failure bit map as a target for the failure analysis method.

7. The failure analysis method according to claim 2, further comprising the step of:

(s) on the basis of a result of extraction in said step (j), calculating periodicity in frequency of occurrence of failure bits in a column direction.

8. The failure analysis method according to claim 3, further comprising the step of:

(t) on the basis of a result of extraction in said step (m), calculating periodicity in frequency of occurrence of failure bits in a row direction.

9. The failure analysis method according to claim 7, further comprising the step of:

(u) removing failure bits having said periodicity in a column direction from said fail bit map.

10. The failure analysis method according to claim 8, further comprising the step of:

(v) removing failure bits having said periodicity in a row direction from said fail bit map.

11. The failure analysis method according to claim 9, further comprising the step of:

(w) on the basis of remaining failure bits, performing data complement on said fail bit map from which failure bits having said periodicity in a column direction have been removed.

12. The failure analysis method according to claim 10, further comprising the step of:

(x) on the basis of remaining failure bits, performing data complement on said fail bit map from which failure bits having said periodicity in a row direction have been removed.

13. The failure analysis method according to claim 1, further comprising the step of:

(y) prior to said step (a), calculating a proportion of failure bits contained in said fail bit map, wherein

when failure bits have said proportion of not less than a predetermined value, said steps (a) through (x) are omitted.

14. The failure analysis method according to claim 7, further comprising the step of:

(z) classifying said block failure having said periodicity in a column direction on the basis of information indicative of a proportion of failure bits and a distribution of failure bits in said block failure.

15. The failure analysis method according to claim 8, further comprising the step of:

(A) classifying said block failure having said periodicity in a row direction on the basis of information indicative of a proportion of failure bits and a distribution of failure bits in said block failure.